Turing RK1

System on Module

DataSheet

Change History

Version	Date	Changes
1.0	2023-10-24	First version

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1. Overview

Turing RK1 is a compact SoM powered by Rockchip 3588, a high-performance low-power AIoT processor that integrates quad-core Cortex-A76 and quad-core Cortex-A55. Capable of delivering up to 6 TOPS AI performance, Turing RK1 targets a wide range of applications, including ARM-based PCs, Edge Computing devices, personal mobile internet devices, and other digital multimedia applications.

2. Main Features

- Excellent video processing capabilities
  - 8Kp60 video decoding (H.264/H.265/VP9)
  - 8Kp30 video encoding (H.264/H.265)
  - JPEG encoding and decoding
- Robust image processing capabilities
  - High Dynamic Range (HDR)
  - 3A
  - LSC
  - 3DNR, 2DNR
  - Sharpening
  - Dehaze
  - Fisheye correction
  - Gamma correction
  - Image preprocessor and postprocessor
- Strong AI performance
  - 6 TOPS
  - INT4/INT8/INT16/FP16
  - TensorFlow/MXNet/PyTorch/Caffe
- High-speed interfaces: PCIe 3.0 x4 lanes + PCIe 2.1 x1 lane

3. Technical Specifications

Technical items		Specifications
General	CPU	Quad-core Cortex-A76 (2.4 GHz) + Quad-core Cortex-A55, Neon and FPU
	GPU	Arm Mali-G610 MP4 with support for OpenGL ES3.2, OpenCL 2.2, Vulkan1.2
	NPU	RK NN, 6 TOPS NPU with support for TensorFlow, Caffe, TFLite, PyTorch, ONNX NN, Android NN
	Memory	8 GB, 16 GB, or 32 GB 64-bit LPDDR4X
	Storage	32 GB eMMC 5.1 flash storage
	Supported OS	Buildroot Linux,Ubuntu 22.04
	Supply power	5 V DC
Interfaces	Display	1x HDMI interface + 1x DP/eDP combo interface, up to 7680 x 4320@60 Hz for HDMI and DP, 3840 x 2160@60 Hz for eDP, 1 MIPI DPHY 2.0 interface
	Camera	3x 4-lane or 5x 2-lane MIPI CSI interfaces @ 2.5 Gbps/lane
	Network	10/100/1000 BASE-T
	USB	1x USB 3.0 (Gen1), 3x USB 2.0
	PCIe	PCIe 3.0 x4 + PCIe 2.1 x1
	Others	• UART DEBUG x1, UART+flow control x2 • SPI x2 • I^2C x3 • CAN x1 • I^2S x2 • SD 4.0, SDHOST 4.0, and SDIO 3.0 • PWM x3, GPIO x15
Mechanical	Connector	260-pin SO-DIMM edge connector, compatible with Jetson Nano/TX2/NX/Orin
	Dimensions	69.6 mm x 45 mm
Environment	Temperature	• Operating: 0°C to 80°C • Storage: -20°C to 85°C
	Relative humidity	• Operating: 10% to 90% • Storage: 5% to 95%

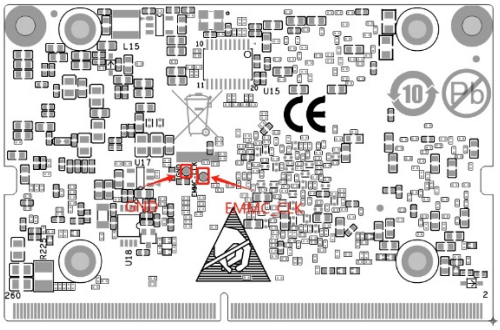
4. Functional Description

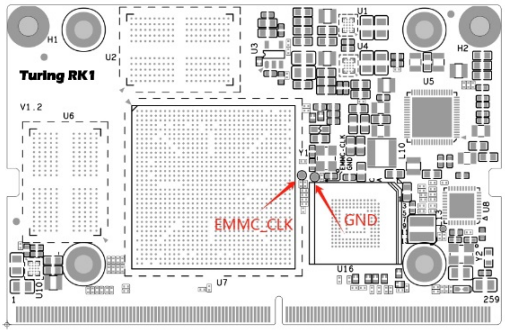
4.1 Microprocessor

- Quad-core ARM Cortex-A76 MPCore processor and quad-core ARM Cortex-A55 MPCore processor, both are high-performance, low-power and cached application processors
- DSU (DynamIQ Shared Unit) comprises the L3 memory system, control logic, and external interfaces to support a DynamIQ cluster
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- TrustZone technology support
- Integrated 64KB L1 instruction cache, 64KB L1 data cache and 512KB L2 cache for each Cortex-A76
- Integrated 32KB L1 instruction cache, 32KB L1 data cache and 128KB L2 cache for each Cortex-A55
- Quad-core Cortex-A76 and Quad-core Cortex-A55 share 3MB L3 cache
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenarios:
  - PD_CPU_0: 1st Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_1: 2nd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_2: 3rd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_3: 4th Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_4: 1st Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_5: 2nd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_6: 3rd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_7: 4th Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
- Three isolated voltage domains to support DVFS, one for A76_0 and A76_1, one for A76_2and A76_3, the other for DSU and Cortex-A55

4.2 Memory Organization

- Internal on-chip memory
  - BootRom
    - Support system boot from the following interfaces:
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB OTG interface
  - Share Memory in the voltage domain of VD_LOGIC
  - PMU SRAM in VD_PMU for low power application
  - Physical method enter Maskrom mode: Shorting the following two pads , Then power on , you'll be forced into Maskrom mode





- External off-chip memory
  - Dynamic Memory Interface
    - Compatible with JEDEC standards LPDDR4/LPDDR4X/LPDDR5
    - Support four channels, 16 bits data widths for each channel
    - Support up to 2 ranks (chip selects) for each channel
    - Totally up to 32 GB address space
    - Low power modes, such as power-down and self-refresh for SDRAM
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification
    - Backward compliant with eMMC 4.51 and earlier versions specification
    - Support HS400, HS200, DDR50 and legacy operating modes
    - Support three data bus widths: 1 bit, 4 bits, and 8 bits
  - SD/MMC Interface
    - Compatible with SD3.0, MMC ver4.51
    - Data bus width is 4 bits
  - Flexible Serial Flash Interface
    - Support transferring data from/to serial flash device
    - Support 1 bit, 2 bits or 4 bits data bus width
    - Support 2 chips select

4.3 System Components

- MCU (microcontroller unit)
  - Three Cortex-M0 MCUs inside RK3588:
    - MCU in VD_PMU integrate 16KB Cache and 16KB TCM
    - MCU in VD_NPU integrate 16KB Cache and 64KB TCM
    - MCU in PD_CENTER integrate 32KB TCM
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU in VD_PMU(PMU_M0) and PD_CENTER(DDR_M0)
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 18 PLLs to generate all clocks
  - One oscillator with 24 MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different modes

- Support 10 separate voltage domains
- Support 45 separate power domains, which can be powered up/down by software based on different application scenes

- Timer
  - Support 12 secure timers with 64 bits counter and interrupt-based operation
  - Support 18 non-secure timers with 64 bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable
- PWM
  - Support 16 on-chip PWMs (PWM0~PWM15) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provide reference mode and output various duty-cycle waveforms
  - Optimized for IR application for PWM3, PWM7, PWM11, PWM15
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - Watchdog timer (WDT) can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt. If this is not cleared by the service routine by the time a second timeout occurs, then generate a system reset
  - Totally five watchdogs for CPU and MCU
- Interrupt controller
  - Support 12 PPI interrupt sources and 480 SPI interrupt sources input from different components inside RK3588
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support different interrupt priorities for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - Totally three embedded DMA controllers for peripheral system
  - Features of each DMAC:
    - Support 8 channels
    - 32 hardware request from peripherals
    - 2 interrupt output
    - Support TrustZone technology and programmable secure state for each DMA channel
- Secure System
  - Embedded two cipher engines
    - Support Link List Item (LLI) DMA transfer
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher

- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES & TDES cipher, with ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
- Support generating random numbers

- Support keyladder to guarantee key secure
- Support data scrambling for all DDR types
- Support secure OTP
- Support secure debug
- Support secure DFT test
- Support secure OS
- Except CPU, the other masters in the SoC can also support security and non- security mode by software-programmable
- Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
- System SRAM (share memory), part of space is addressed only in security mode
- External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master

- Mailbox
  - Three mailboxes in SoC to service CPU and MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- Decompression
  - Support for decompressing GZIP files
  - Support for decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format
  - Support for decompressing data in DEFLATE format
  - Support for decompressing data in ZLIB format
  - Support Hash32 check in LZ4 decompression process
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

4.4 Video Codec

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC, AV1
  - MMU Embedded
  - Multi-channel decoder in parallel for less resolution
  - H.264 AVC/MVC Main10 L6.0 : 8K@30fps (7680 x 4320)[2]
  - VP9 Profile0/2 L6.1 : 8K@60fps (7680 x 4320)
  - H.265 HEVC/MVC Main10 L6.1 : 8K@60fps (7680 x 4320)
  - AVS2 Profile0/2 L10.2.6 : 8K@60fps (7680 x 4320)

- AV1 Main Profile 8/10bit L5.3. : 4K@60fps (3840 x 2160)
- MPEG-2 up to MP : 1080p@60fps (1920 x 1088)
- MPEG-1 up to MP : 1080p@60fps (1920 x 1088)
- VC-1 up to AP level 3 : 1080p@60fps (1920 x 1088)
- VP8 version2 : 1080p@60fps (1920 x 1088)

- Video Encoder
  - Real-time H.265/H.264 video encoding
  - Support up to 8K@30fps
  - Multi-channel encoder in parallel for less resolution

4.5 JPEG Codec

- JPEG Encoder
  - Baseline (DCT sequential)
  - Encoder size is from 96 x 96 to 8192 x 8192 (67 Mpixels)
  - Up to 90 million pixels per second
  - Embedded four encoder units
- JPEG Decoder
  - Decoder size is from 48 x 48 to 65536 x 65536
  - Support YUV400/YUV411/YUV420/YUV422/YUV440/YUV444
  - Support up to 1080P@280fps, and 560 million pixels per second
  - Support MJPEG
  - Embedded four encoder units

4.6 Neural Process Unit

- Neural network acceleration engine with processing performance up to 6 TOPS
- Include triple NPU core, and support triple core co-work, dual core co-work, and work independently
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation
- Embedded 384KBx3 internal buffer
- Multi-task, multi-scenario in parallel
- Support deep learning frameworks: TensorFlow, Caffe, TFlite, PyTorch, ONNX NN, Android NN, etc.
- One isolated voltage domain to support DVFS

4.7 Graphics Engine

- 3D Graphics Engine
  - ARM Mali-G610 MP4
  - High performance OpenGLES 1.1, 2.0 and 3.2, OpenCL 2.2, Vulkan1.2 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 4x 256 KB size
  - The latest Valhall architecture
  - ARM Frame Buffer Compression (AFBC) 1.3
  - Support Serial Wire debug for embedded MCU
  - One isolated voltage domain to support DVFS

- 2D Graphics Engine
  - Source format: ARGB/RGB888/RGB565/YUV420/YUV422/BPP
  - Destination formats: ARGB/RGB888/RGB565/YUV420/YUV422
  - Max resolution: 8192 x 8192 source, 4096 x 4096 destination
  - Block transfer and transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
  - Arbitrary non-integer scaling ratio, from 1/8 to 8
  - 0, 90, 180, 270 degree rotation, x-mirror, y-mirror & rotation operation
  - ROP2, ROP3, ROP4
  - Support 4k/64k page size MMU
- Image enhancement processor
  - Image format
    - Input data: YUV420/YUV422, semi-planar/planar, UV swap
    - Output data: YUV420/YUV422, semi-planar, UV swap, Tile mode
    - YUV down sampling conversion from 422 to 420
    - Max resolution for dynamic image up to 1920 x 1080
  - De-interlace

4.8 Video Input Interface

- MIPI interface
  - Two MIPI DC (DPHY/CPHY) combo PHY
    - Support to use DPHY or CPHY
    - Each MIPI DPHY V2.0, 4 lanes, 4.5 Gbps per lane
    - Each MIPI CPHY V1.1, 3 lanes, 2.5 Gbps per lane
  - Four MIPI CSI DPHY
    - Each MIPI DPHY V1.2, 2 lanes, 2.5 Gbps per lane
    - Support to combine 2 DPHY together to one 4-lane
  - Support camera input combination
    - 2 MIPI DCPHY + 4 MIPI CSI DPHY (2 lanes), totally support 6 cameras input
    - 2 MIPI DCPHY + 1 MIPI CSI DPHY (4 lanes) + 2 MIPI CSI DPHY (2 lanes), totally support 5 cameras input
    - 2 MIPI DCPHY + 2 MIPI CSI DPHY (4 lanes), totally support 4

cameras input

Table 1: CSI Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
10	MIPI_CSI0_RX_CLK0N	Camera, CSI 0 Clock0–	Input	MIPI D-PHY
12	MIPI_CSI0_RX_CLK0P	Camera, CSI 0 Clock0+	Input	MIPI D-PHY
4	MIPI_CSI0_RX_D0N	Camera, CSI 0 Data 0–	Input	MIPI D-PHY
6	MIPI_CSI0_RX_D0P	Camera, CSI 0 Data 0+	Input	MIPI D-PHY
16	MIPI_CSI0_RX_D1N	Camera, CSI 0 Data 1–	Input	MIPI D-PHY
18	MIPI_CSI0_RX_D1P	Camera, CSI 0 Data 1+	Input	MIPI D-PHY
9	MIPI_CSI0_RX_CLK1N	Camera, CSI 0 Clock1–	Input	MIPI D-PHY

11	MIPI_CSI0_RX_CLK1P	Camera, CSI 0 Clock1+	Input	MIPI D-PHY
3	MIPI_CSI0_RX_D2N	Camera, CSI 0 Data 2–	Input	MIPI D-PHY
5	MIPI_CSI0_RX_D2P	Camera, CSI 0 Data 2+	Input	MIPI D-PHY
15	MIPI_CSI0_RX_D3N	Camera, CSI 0 Data 3–	Input	MIPI D-PHY
17	MIPI_CSI0_RX_D3P	Camera, CSI 0 Data 3+	Input	MIPI D-PHY
28	MIPI_CSI1_RX_CLK0N	Camera, CSI 1 Clock0–	Input	MIPI D-PHY
30	MIPI_CSI1_RX_CLK0P	Camera, CSI 1 Clock0+	Input	MIPI D-PHY
22	MIPI_CSI1_RX_D0N	Camera, CSI 1 Data 0–	Input	MIPI D-PHY
24	MIPI_CSI1_RX_D0P	Camera, CSI 1 Data 0+	Input	MIPI D-PHY
34	MIPI_CSI1_RX_D1N	Camera, CSI 1 Data 1–	Input	MIPI D-PHY
36	MIPI_CSI1_RX_D1P	Camera, CSI 1 Data 1+	Input	MIPI D-PHY
27	MIPI_CSI1_RX_CLK1N	Camera, CSI 1 Clock1–	Input	MIPI D-PHY
29	MIPI_CSI1_RX_CLK1P	Camera, CSI 1 Clock1+	Input	MIPI D-PHY
21	MIPI_CSI1_RX_D2N	Camera, CSI 1 Data 2–	Input	MIPI D-PHY
23	MIPI_CSI1_RX_D2P	Camera, CSI 1 Data 2+	Input	MIPI D-PHY
33	MIPI_CSI1_RX_D3N	Camera, CSI1 Data 3–	Input	MIPI D-PHY
35	MIPI_CSI1_RX_D3P	Camera, CSI 1 Data 3+	Input	MIPI D-PHY
52	MIPI_DPHY0_RX_CLKN	Camera, DPHY 0 Clock–	Input	MIPI D-PHY
54	MIPI_DPHY0_RX_CLKP	Camera, DPHY 0 Clock+	Input	MIPI D-PHY
46	MIPI_DPHY0_RX_D0N	Camera, DPHY 0 Data 0–	Input	MIPI D-PHY
48	MIPI_DPHY0_RX_D0P	Camera, DPHY 0 Data 0+	Input	MIPI D-PHY
58	MIPI_DPHY0_RX_D1N	Camera, DPHY 0 Data 1–	Input	MIPI D-PHY
60	MIPI_DPHY0_RX_D1P	Camera, DPHY 0 Data 1+	Input	MIPI D-PHY
40	MIPI_DPHY0_RX_D2N	Camera, DPHY 0 Data 2–	Input	MIPI D-PHY
42	MIPI_DPHY0_RX_D2P	Camera, DPHY 0 Data 2+	Input	MIPI D-PHY
64	MIPI_DPHY0_RX_D3N	Camera, DPHY 0 Data 3–	Input	MIPI D-PHY
66	MIPI_DPHY0_RX_D3P	Camera, DPHY 0 Data 3+	Input	MIPI D-PHY

Table 2: Camera Control Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
213	I2C3_SCL_M0	Camera I2C Clock.	Bidir	Open Drain – 3.3V
215	I2C3_SDA_M0	Camera I2C Data.	Bidir	Open Drain – 3.3V
116	MIPI_CAM3_CLKOUT	Camera 3 Reference Clock	Output	CMOS – 1.8V
114	MIPI_CAM3_PDN_L	Camera 3 Power down or GPIO	Output	CMOS – 1.8V
122	MIPI_CAM4_CLKOUT	Camera 4 Reference Clock	Output	CMOS – 1.8V
120	MIPI_CAM4_PDN_L	Camera 4 Power down or GPIO	Output	CMOS – 1.8V

- DVP interface
  - One 8/10/12/16-bit standard DVP interface, up to 150 MHz input data
  - Support BT.601/BT.656 and BT.1120 VI interface
  - Support the polarity of pixel_clk, hsync, vsync configurable

- HDMI RX interface
  - Single-port HDMI 2.0 RX PHY, 4 lanes, no sideband channels
  - Data rate support in HDMI 2.0 mode
    - 6 Gbps down to 3.4 Gbps
  - Data rate support in HDMI 1.4 mode
    - 3.4 Gbps down to 250 Mbps
  - HDMI 2.0 video formats
    - TMDS Scrambler to enable support for 2160p@60 Hz with RGB/YCbCr4:4:4 or YCbCr4:2:2
    - Supports YCbCr 4:2:0 to enable 2160p@60 Hz at lower HDMI link speeds
  - HDMI 1.4b video formats
    - All CEA-861-E video formats up to 1080p@120 Hz
    - HDMI 1.4b 4K x 2K video formats (3840 x 2160p@24 Hz/25 Hz/30 Hz and 4096 x 2160p@24 Hz)
    - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
  - Support HDCP2.3 and HDCP1.4

4.9 Image Signal Processor

- Video Capture (VICAP)
  - Support BT601, BT656, BT1120
  - Support receiving six interfaces of MIPI CSI/DSI, up to four IDs for each interface
  - Support five CSI data formats: RAW8/10/12/14, YUV422
  - Support three modes of HDR: virtual channel mode, identification code mode, line counter mode
  - Support RAW data through to ISP0/1
- Maximum input
  - 48M: 8064 x 6048@15 dual ISP
  - 32M: 6528 x 4898@30 dual ISP
  - 16M: 4672 x 3504@30 single ISP
- 3A: include AE/Histogram, AF, AWB statistics output
- FPN: Fixed Pattern Noise removal
- BLC: Black Level Correction
- DPCC: Static/Dynamic defect pixel cluster correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens shading correction
- Bayer-2DNR: Spatial Bayer-raw De-noising
- Bayer-3DNR: Temporal Bayer-raw De-noising
- CAC: Chromatic Aberration Correction
- HDR: 3-Frame Merge into High-Dynamic Range
- DRC: HDR Dynamic Range Compression, Tone mapping
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction
- CCM/CSM: Color correction matrix; RGB2YUV etc
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and Effect enhancement
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion only in the horizontal direction

- YUV-2DNR: Spatial YUV De-noising
- Sharp: Image Sharpening and boundary filtering
- CMSK: privacy mask
- GAIN: image local gain
- Support multi-sensor reuse ISP
- FishEye Correction (FEC)
  - Input mode and data format
    - Support RASTER: YUV422SP, YUV422I, YUV420SP
  - Output mode and data format
    - RASTER: YUV422SP, YUV422I, YUV420SP
    - FBCE: YUV422SP, YUV420SP
  - Support 16 x 8, 32 x 16 two densities
  - Support up to 4 times reduction factor
  - Resolution 128 x 128~4095 x 4095
  - Y Interpolation: Bicubic; C Interpolation: Biliner

4.10 Display Interface

- HDMI TX interface
  - Support one HDMI TX
  - Support 1/2/4 lanes for each interface
  - Support all the data rates: 3, 6, 8, 10 and 12 Gbps
  - Support up to 7680 x 4320@60 Hz
  - Support RGB/YUV (up to 10 bits) format
  - Support DSC 1.2a
  - Support HDCP2.3
- DP/eDP TX interface
  - Support one DP/eDP combo interface
  - Support 1/2/4 lanes for each interface
  - Support 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps for DP
  - Support 1.62 Gbps, 2.7 Gbps, 5.4 Gbps for eDP
  - Support up to 7680 x 4320@60 Hz for DP, 8192 x 4320@30 Hz for eDP
  - Support RGB/YUV (up to 10 bits) format for DP
  - Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format for eDP
  - Support Single Stream Transport (SST) for DP
  - Support HDCP 2.3/HDCP 1.3 for DP, HDCP1.3 for eDP
- MIPI DSI interface
  - Support 1 MIPI DPHY 2.0 interface
  - Support 4 data lanes and 4.5 Gbps maximum data rate per lane
  - Support max resolution 4K@60 Hz
  - Support dual MIPI display: left-right mode
  - Support RGB (up to 10 bits) format
  - Support DSC 1.1/1.2a
- BT.1120 video output interface
  - Support up to 1920 x 1080@60 Hz
  - Support RGB (up to 8 bits) format
  - Up to 150 MHz data rate

Table 3: DSI Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
76	MIPI_DPHY0_TX_CLKN	MIPI_DPHY0_TX Clock–	Output	MIPI D-PHY
78	MIPI_DPHY0_TX_CLKP	MIPI_DPHY0_TX Clock+	Output	MIPI D-PHY
70	MIPI_DPHY0_TX_D0N	MIPI_DPHY0_TX Data 0–	Output	MIPI D-PHY
72	MIPI_DPHY0_TX_D0P	MIPI_DPHY0_TX Data 0+	Output	MIPI D-PHY
82	MIPI_DPHY0_TX_D1N	MIPI_DPHY0_TX Data 1–	Output	MIPI D-PHY
84	MIPI_DPHY0_TX_D1P	MIPI_DPHY0_TX Data 1+	Output	MIPI D-PHY

Table 4: DP/eDP/HDMI Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
39	TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1- /Display Port 0 Lane 0-	Output	DP/eDP
41	TYPEC0_SSRX1P/DP0_TX0P	TYPEC0_SSRX1+/Display Port 0 Lane 0+	Output	DP/eDP
45	TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1-/Display Port 0 Lane 1–	Output	DP/eDP
47	TYPEC0_SSTX1P/DP0_TX1P	TYPEC0_SSTX1+/Display Port 0 Lane 1+	Output	DP/eDP
51	TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2-/Display Port 0 Lane 2–	Output	DP/eDP
53	TYPEC0_SSRX2P/DP0_TX2P	TYPEC0_SSRX2+/Display Port 0 Lane 2+	Output	DP/eDP
57	TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2-/Display Port 0 Lane 3–	Output	DP/eDP
59	TYPEC0_SSTX2P/DP0_TX3P	TYPEC0_SSTX2+/Display Port 0 Lane 3+	Output	DP/eDP
90	TYPEC0_SBU2/DP0_AUXN	TYPEC0_ SBU2/Display Port 0 Aux–	Bidir	DP/eDP
92	TYPEC0_SBU1/DP0_AUXP	TYPEC0_ SBU1/Display Port 0 Aux+	Bidir	DP/eDP
88	DP0_HPDIN_M1	Display Port 0 Hot Plug Detect	Input	Open Drain – 1.8V
63	HDMI_TX2_N	HDMI Lane 2–	Output	HDMI
65	HDMI_TX2_P	HDMI Lane 2+	Output	HDMI
69	HDMI_TX1_N	HDMI Lane 1–	Output	HDMI
71	HDMI_TX1_P	HDMI Lane 1+	Output	HDMI
75	HDMI_TX0_N	HDMI Lane 0–	Output	HDMI
77	HDMI_TX0_P	HDMI Lane 0+	Output	HDMI
81	HDMI_TXC_N	HDMI Clk Lane–	Output	HDMI
83	HDMI_TXC_P	HDMI Clk Lane+	Output	HDMI
98	HDMI_DDC_SDA_POL	HDMI DDC SDA	Bidir	Open-Drain, 3.3V
100	HDMI_DDC_SCL_POL	HDMI DDC SCL	Output	Open-Drain, 3.3V
96	HDMI_HPD	HDMI Hot Plug Detect	Input	Open Drain – 1.8V
94	HDMI_CEC	HDMI CEC	Bidir	Open Drain – 3.3V

4.11 Video output processor

- Video ports
  - Video Port0, max output resolution: 7680 x 4320@60 Hz
  - Video Port1, max output resolution: 4096 x 2304@60 Hz
  - Video Port2, max output resolution: 4096 x 2304@60 Hz
  - Video Port3, max output resolution: 1920 x 1080@60 Hz
- Cluster 0/1/2/3
  - Max input and output resolution 4096 x 2304
  - Support AFBCD
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 4~1/4
  - Support rotation
- ESMART 0/1/2/3
  - Max input and output resolution 4096 x 2304
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 8~1/8
  - Support 4 regions
  - Overlay
    - Support up to 8 layers overlay: 4 cluster/4 esmart
    - Support RGB/YUV domain overlay
- Post process
  - HDR
    - HDR10/HDR HLG
    - HDR2SDR/SDR2HDR
  - 3D-LUT/P2I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR
- Write back
  - Format: ARGB8888/RGB888/RGB565/YUV420
  - Max resolution: 1920 x 1080

4.12 Audio Interface

- I^2S0/I^2S1 with 8 channels
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16 bits to 32 bits
  - Sample rate up to 192 KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I^2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
  - I^2S, PCM and TDM mode cannot be used at the same time
- I^2S2/I^2S3 with 2 channels
  - Up to 2 channels for TX and 2 channels for RX path
  - Audio resolution from 16 bits to 32 bits
  - Sample rate up to 192 KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I^2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I^2S and PCM cannot be used at the same time

- SPDIF0/SPDIF1
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support bi-phase format stereo audio data output
  - Support 16- to 31-bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16-, 20-, 24-bit audio data transfer in linear PCM mode
  - Support non-linear PCM transfer
- PDM0/PDM1
  - Up to 8 channels
  - Audio resolution from 16 bits to 24 bits
  - Sample rate up to 192 KHz
  - Support PDM master receive mode
- Digital Audio Codec
  - Support 2 channels digital DAC
  - Support I^2S/PCM interface, master and slave mode
  - Support 16-bit sample resolution
  - Support three modes of mixing for every digital DAC channel
  - Support volume control
- VAD (Voice Activity Detection)
  - Support read voice data from I^2S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

Table 5: I^2S Audio Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
199	I2S0_SCLK	I2S Audio Clock	Bidir	CMOS – 1.8V
197	I2S0_LRCK	I2S Audio Left/Right Clock	Bidir	CMOS – 1.8V
193	I2S0_SDO0	I2S Audio Data Out	Output	CMOS – 1.8V
195	I2S0_SDI0	I2S Audio Data In	Input	CMOS – 1.8V
226	I2S2_SCLK_M0_BT	I2S BT Clock	Bidir	CMOS – 1.8V
224	I2S2_LRCK_M0_BT	I2S BT Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S2_SDO_M0_BT	I2S BT Data Out	Output	CMOS – 1.8V
222	I2S2_SDI_M0_BT	I2S BT Data In	Input	CMOS – 1.8V

4.13 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus width

Table 6: SDIO Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
229	SDMMC_CLK	SD Card or SDIO Clock	Output	CMOS – 1.8V/3.3V
227	SDMMC_CMD	SD Card or SDIO Command	Bidir	CMOS – 1.8V/3.3V
219	SDMMC_DAT0	SD Card or SDIO Data 0	Bidir	CMOS – 1.8V/3.3V
221	SDMMC_DAT1	SD Card or SDIO Data 1	Bidir	CMOS – 1.8V/3.3V
223	SDMMC_DAT2	SD Card or SDIO Data 2	Bidir	CMOS – 1.8V/3.3V

225	SDMMC_DAT3	SD Card or SDIO Data 3	Bidir	CMOS – 1.8V/3.3V

- GMAC 10/100/1000M Ethernet controller
  - Support two Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex

operation Table 7: Gigabit Ethernet Pin

Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
184	GBE_MDI0_N	GbE Transformer Data 0–	Bidir	MDI
186	GBE_MDI0_P	GbE Transformer Data 0+	Bidir	MDI
190	GBE_MDI1_N	GbE Transformer Data 1–	Bidir	MDI
192	GBE_MDI1_P	GbE Transformer Data 1+	Bidir	MDI
196	GBE_MDI2_N	GbE Transformer Data 2–	Bidir	MDI
198	GBE_MDI2_P	GbE Transformer Data 2+	Bidir	MDI
202	GBE_MDI3_N	GbE Transformer Data 3–	Bidir	MDI
204	GBE_MDI3_P	GbE Transformer Data 3+	Bidir	MDI
188	GBE_LED_ACT	Ethernet Activity LED (Green)	Output	-
194	GBE_LED_LINK	Ethernet Link LED (Yellow)	Output	-

- USB 3.0
  - Embedded two USB 3.0 OTG interfaces which combo with DP TX (USB3OTG_0 and USB3OTG_1)
  - Embedded one USB 3.0 Host interface which combos with Combo PIPE PHY2 (USB3OTG_2)
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB3.0, up to 8 Gbps bandwidth
  - Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  - LPM protocol in USB 2.0 (exclude USB3OTG_2) and U0, U1, U2, and U3 states for USB 3.0
  - USB3.0 Device Features
    - Up to 10 IN endpoints, including control endpoint 0
    - Up to 6 OUT endpoints, including control endpoint 0
    - Up to 16 endpoint transfer resources, each one for each endpoint
    - Flexible endpoint configuration for multiple applications/USB set-configuration modes
    - Hardware handles ERDY and burst
    - Stream-based bulk endpoints with controller automatically initiating data movement
    - Isochronous endpoints with isochronous data in data buffers

- Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support

- USB 3.0 xHCI Host Features
  - Support up to 64 devices
  - Support one interrupter
  - Support one USB2.0 port (exclude USB3OTG_2) and one Super-Speed port
  - Support standard or open-source xHCI and class driver
- USB 3.0 Dual-Role Device (DRD) Features
  - Static Device Operation
  - Static Host Operation
  - USB3.0/USB2.0 OTG A device and B device basing on ID, USB3OTG_2 only support USB3.0
  - Not Support USB3.0/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  - USB2.0 PHY support Battery Charge detection
  - USB3OTG_0 and USB3OTG_1 support USB Type-C and DP Alt Mode
  - USB3OTG_2 PHY combos with PCIE and SATA

Table 8: USB3.0 GEN1 Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
161	TYPEC1_SSRX1N	USB SS Receive– (USB 3.0 Ctrl #0)	Input	USB SS PHY
163	TYPEC1_SSRX1P	USB SS Receive+ (USB 3.0 Ctrl #0)	Input	USB SS PHY
166	TYPEC1_SSTX1N	USB SS Transmit– (USB 3.0 Ctrl #0)	Output	USB SS PHY
168	TYPEC1_SSTX1P	USB SS Transmit+ (USB 3.0 Ctrl #0)	Output	USB SS PHY

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Support two USB 2.0 Hosts
  - Supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI),

Revision 1.0a Table 9: USB2.0 Pin Descriptions

Pin #	**Pin Name**	**Signal Description**	**Direction**	**Pin Type**
109	USB0_OTG_D_N	USB2.0 Port 0 Data–	Bidir	USB PHY
111	USB0_ OTG_D_P	USB2.0 Port 0 Data+	Bidir	USB PHY
115	USB1_ OTG_D_N	USB 2.0 Port 1 Data–	Bidir	USB PHY
117	USB1_ OTG_D_P	USB 2.0 Port 1 Data+	Bidir	USB PHY
121	USB2_HOST0_D_N	USB 2.0 Port 2 Data–	Bidir	USB PHY
123	USB2_HOST0_D_P	USB 2.0 Port 2 Data+	Bidir	USB PHY

- Combo PIPE PHY Interface
  - Support three Combo PIPE PHYs with PCIe2.1/SATA3.0/USB3.0 controller
- Combo PIPE PHY0 supports one of the following interfaces:

- SATA
- PCIe2.1

- Combo PIPE PHY1 supports one of the following interfaces:
  - SATA
  - PCIe2.1
- Combo PIPE PHY2 supports one of the following interfaces:
  - SATA
  - PCIe2.1
  - USB3.0
- PCIe2.1 Interface
  - Compatible with PCI Express Base Specification Revision 2.1
  - Support one lane for each PCIe2.1 interface
  - Support Root Complex (RC) only

Support 5 Gbps data rate Table 10: PCIE2.1 Pin Descriptions**Pin #**	**Pin Name**	**Signal Description**	**Direction**	**Pin Type**
167	PCIE20_2_RXN	PCIe #1 Receive 0– (PCIe Ctrl #2 Lane 0)	Input	PCIe PHY.
169	PCIE20_2_RXP	PCIe #1 Receive 0+ (PCIe Ctrl #2 Lane 0)	Input	PCIe PHY
172	PCIE20_2_TXN	PCIe #2 Transmit 0– (PCIe Ctrl #2 Lane 0)	Output	PCIe PHY
174	PCIE20_2_TXP	PCIe #2 Transmit 0+ (PCIe Ctrl #2 Lane 0)	Output	PCIe PHY
183	PCIEX1_1_RST_M1	PCIe #1 Reset (PCIe Ctrl #2). 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain – 3.3V
182	PCIEX1_1_CLKREQ_M1	PCIe #1 Clock Request (PCIe Ctrl #2). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
173	PCIE20_2_REFCLKN	PCIe #2 Reference Clock– (PCIe Ctrl #2)	Output	PCIe PHY
175	PCIE20_2_REFCLKP	PCIe #2 Reference Clock+ (PCIe Ctrl #2)	Output	PCIe PHY
179	PCIEX1_1_WAKE_M1	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Input	Open Drain – 3.3V

- SATA interface
  - Compatible with Serial ATA 3.1 and AHCI revision 1.3.1
  - Support eSATA
  - Support one port for each SATA interface
  - Support 6 Gbps data rate
- PCIe3.0 interface
  - Compatible with PCI Express Base Specification Revision 3.0
  - Support dual operation modes: Root Complex (RC) and End Point (EP)
  - Support data rates: 2.5 Gbps (PCIe1.1), 5 Gbps (PCIe2.1), 8 Gbps (PCIe3.0)
  - Support aggregation and bifurcation with 1x 4 lanes, 2x 2 lanes, 4x 1 lanes and 1x 2

lanes + 2x 1 lanes

Table 11: PCIE3.0 Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
131	PCIE30_PORT0_RX0N	PCIe #0 Receive 0– (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
133	PCIE30_PORT0_RX0P	PCIe #0 Receive 0+ (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
137	PCIE30_PORT0_RX1N	PCIe #0 Receive 1– (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
139	PCIE30_PORT0_RX1P	PCIe #0 Receive 1+ (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
134	PCIE30_PORT0_TX0N	PCIe #0 Transmit 0– (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
136	PCIE30_PORT0_TX0P	PCIe #0 Transmit 0+ (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
140	PCIE30_PORT0_TX1N	PCIe #0 Transmit 1– PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
142	PCIE30_PORT0_TX1P	PCIe #0 Transmit 1+ (PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
181	PCIE30X4_RST_M1	PCIe #0 Reset (PCIe Ctrl #0). 4.7kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
180	PCIE30X4_CLKREQ_M1	PCIe #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
179	PCIE30X4_1_WAKE_M1	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Input	Open Drain – 3.3V
160	PCIE30_REFCLKN_SLOT	PCIe #0 Reference Clock–	Output	PCIe PHY
162	PCIE30_REFCLKP_SLOT	PCIe #0 Reference Clock+	Output	PCIe PHY

- SPI interface
  - Support 5 SPI Controllers (SPI0-SPI4)
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

Table 12: SPI Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
91	SPI0_CLK_M2	SPI 0 Clock	Bidir	CMOS – 1.8V
89	SPI0_MOSIM2	SPI 0 Master Out / Slave In	Bidir	CMOS – 1.8V
93	SPI0_MISO_M2	SPI 0 Master In / Slave Out	Bidir	CMOS – 1.8V
95	SPI0_CS0_M2	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V
97	SPI0_CS1_M2	SPI 0 Chip Select 1	Bidir	CMOS – 1.8V
106	SPI2_CLK_M1	SPI 1 Clock	Bidir	CMOS – 1.8V
104	SPI2_MOSI_M1	SPI 1 Master Out / Slave In	Bidir	CMOS – 1.8V
108	SPI2_MISO_M1	SPI 1 Master In / Slave Out	Bidir	CMOS – 1.8V
110	SPI2_CS0_M1	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V
112	SPI2_CS1_M1	SPI 1 Chip Select 1	Bidir	CMOS – 1.8V

- I^2C Master controller
  - Support 9 I^2C Master (I^2C0-I^2C8)
  - Support 7-bit and 10-bit address mode
  - Software programmable clock frequency

- Data on the I²C-bus can be transferred at rates of up to 100 Kbps in the Standard-mode, up to 400 Kbps in the Fast-mode

Table 13: I²C Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
185	I2C5_SCL_M3	General I2C 5 Clock. 2.2kΩ pull-up to 3.3V on module.	Bidir	Open Drain – 3.3V
187	I2C5_SDA_M3	General I2C 5 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
189	I2C4_SCL_M1	General I2C 4 Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
191	I2C4_SDA_M1	General I2C 4 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
232	I2C7_SCL_M0_CODEC	CODEC I2C 7 Clock. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
234	I2C7_SCL_M0_CODEC	CODEC I2C 7 Data. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
213	I2C3_SCL_M0	General I2C 3 Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
215	I2C3_SDA_M0	General I2C 3 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V

- UART interface
  - Support 10 UART interfaces (UART0-UART9)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support transmitting or receiving 5-bit, 6-bit, 7-bit, and 8-bit serial data
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clocks for UART operation to get up to 4 Mbps baud rate
  - Support auto flow control mode for all UART interfaces

Table 14: UART Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
99	UART6_TXD_M0	UART #6 Transmit	Output	CMOS – 1.8V
101	UART6_RXD_M0	UART #6 Receive	Input	CMOS – 1.8V
103	UART6_RTSn_M0	UART #6 Request to Send	Output	CMOS – 1.8V
105	UART6_CTSn_M0	UART #6 Clear to Send	Input	CMOS – 1.8V
203	UART9_TXD_M0_BT	UART #9 Transmit	Output	CMOS – 1.8V
205	UART9_RXD_M0_BT	UART #9 Receive	Input	CMOS – 1.8V
207	UART9_RTSn_M0_BT	UART #9 Request to Send	Output	CMOS – 1.8V
209	UART9_CTSn_M0_BT	UART #9 Clear to Send	Input	CMOS – 1.8V
236	UART2_TXD_M0_DEBUG	UART #2 Transmit	Output	CMOS – 1.8V
238	UART2_RXD_M0_DEBUG	UART #2 Receive	Input	CMOS – 1.8V

- CAN Bus
  - Support 1 CAN bus
  - Support CAN 2.0B protocol
  - Support transmitting or receiving CAN standard frame
  - Support transmitting or receiving CAN extended frame
  - Support transmitting or receiving data frame, remote frame, overload frame, error frame, and frame interval

Table 15: CAN Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
145	CAN2_TX_M0	CAN PHY Transmit	Output	CMOS – 3.3V
143	CAN2_RX_M0	CAN PHY Receive	Input	CMOS – 3.3V

4.14 Others

- Multiple groups of GPIOs
  - All GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable

drive strength Table 16: GPIO Pin

Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
87	GPIO3_C1	GPIO #3_C1 or USB 0 VBUS Enable #0	Bidir	CMOS – 1.8V
118	GPIO3_C6	GPIO #3_C6	Bidir	CMOS – 1.8V
124	GPIO3_C7	GPIO #3_C7	Bidir	CMOS – 1.8V
126	GPIO3_D0/PWM8_M2	GPIO #33_D0/PWM8_M2 or Pulse Width Modulator	Bidir	CMOS – 1.8V
127	GPIO3_D1/PWM9_M2	GPIO #3_D1/PWM9_M2 or Pulse Width Modulator	Bidir	CMOS – 1.8V
128	GPIO3_D2	GPIO #3_D2	Bidir	CMOS – 1.8V
130	GPIO3_D4	GPIO #3_D4	Bidir	CMOS – 1.8V
206	GPIO3_D3/PWM10_M2	GPIO #3_D3 or Pulse Width Modulator	Bidir	CMOS – 1.8V
208	SDMMC_DET/GPIO0_A4	GPIO #0_A4 or SDMMC_DET	Bidir	CMOS – 1.8V
211	GPIO4_B1	GPIO #4_B1	Bidir	CMOS – 1.8V
212	GPIO4_B3	GPIO #4_B3	Bidir	CMOS – 1.8V
216	GPIO1_A6	GPIO #1_A6	Bidir	CMOS – 1.8V
218	GPIO1_A4	GPIO #1_A4	Bidir	CMOS –

				1.8V
228	GPIO1_A3/PWM1_M2	GPIO #1_A3 or Pulse Width Modulator	Bidir	CMOS – 1.8V
230	GPIO1_A2/PWM0_M2	GPIO #1_A2 or Pulse Width Modulator	Bidir	CMOS – 1.8V

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support up to 7 channels TS-ADC, the temperature criteria of each channel can be configurable
  - -40~125°C temperature range and 1°C temperature resolution
- Successive approximation register ADC (SAR ADC)
  - 12-bit resolution
  - Up to 1 MS/s sampling rate
  - Eight single-ended input channels
- OTP
  - Support 32 Kbit address space and the higher 4 Kbit address space is non-secure part
  - Support read and program word mask in secure model
  - Support maximum 32-bit OTP program operation
  - Support maximum 16-word OTP read operation
  - Program and Read state can be read
  - Program fail address record
- Package Type
  - FCBGA1088L (body: 23 mm x 23 mm; ball size: 0.36 mm; ball pitch: 0.65 mm)

5. Power and System Management

5.1 Power and System Management

VIN must be supplied by the carrier board that the module is designed to connect to. All interfaces are referenced to on- module voltage rails, additional I/O voltage is not required to be supplied to the module.

Table 17: Power and System Control Pin Descriptions

Pin #	Pin Name	Signal Description	Direction	Pin Type
251 252 253 254 255 256 257 258 259 260	VDD_IN	Main power – Supplies PMIC and other registers	Input	5.0V
235	RTC_BAT_IN	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	1.65V-5.5V
237	POWER_EN	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 45 kΩ pullup is in the PMIC.	Input	CMOS – 5.0V
239	SYS_RESET*	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies.	Bidir	Open Drain
210	CLK_32K_OUT	Sleep/Suspend clock	Output	CMOS –1.8V
214	FORCE_RECOVERY*	Force Recovery strap pin	Input	CMOS –1.8V

5.2 Power Management Controller (PMC)

The PMC power management features enable both high speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I^2C, RTC, USB) which can wake the system from deep sleep state. The PMC enables aggressive power-gating capabilities on idle modules and integrates specific logic to maintain defined states and control power domains during sleep and deep sleep modes.

5.3 Resets

If you assert reset, the Turing RK1 and onboard storage will be reset. This signal is also used for baseboard power sequencing.

5.4 PMIC_BBAT

An optional backup battery can be attached to the VCC_RTC module input to maintain the module RTC when VIN is not present. This pin is connected directly to the onboard PMIC. Details of the types of backup cells that optionally can be connected are found in the PMIC manufacturer's data sheet. When a backup cell is connected to the PMIC, the RTC retains its contents and can be configured to charge the backup cell as well. RTC accuracy is 2 seconds/day in typical room temperature only.

The following backup cells may be attached to this pin:

- Super capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells
  The backup cells must provide a voltage in the range 2.5 V to 3.5 V.

5.5 Power Sequencing

Turing RK1 is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the SYS_RESET* signal (when deasserted) is used to indicate when the carrier board can power on. The following sections provide an overview of the power sequencing steps between the carrier board and Turing RK1. The Turing RK1 and the product carrier board must be power sequenced properly to avoid potential damage to

components on either the module or the carrier board system.

5.5.1 Power Up

During power-up, the carrier board must wait until the signal SYS_RESET* is deasserted from the Turing RK1 before enabling its power; the Turing RK1 deasserts the SYS_RESET* signal to enable the complete system to boot.

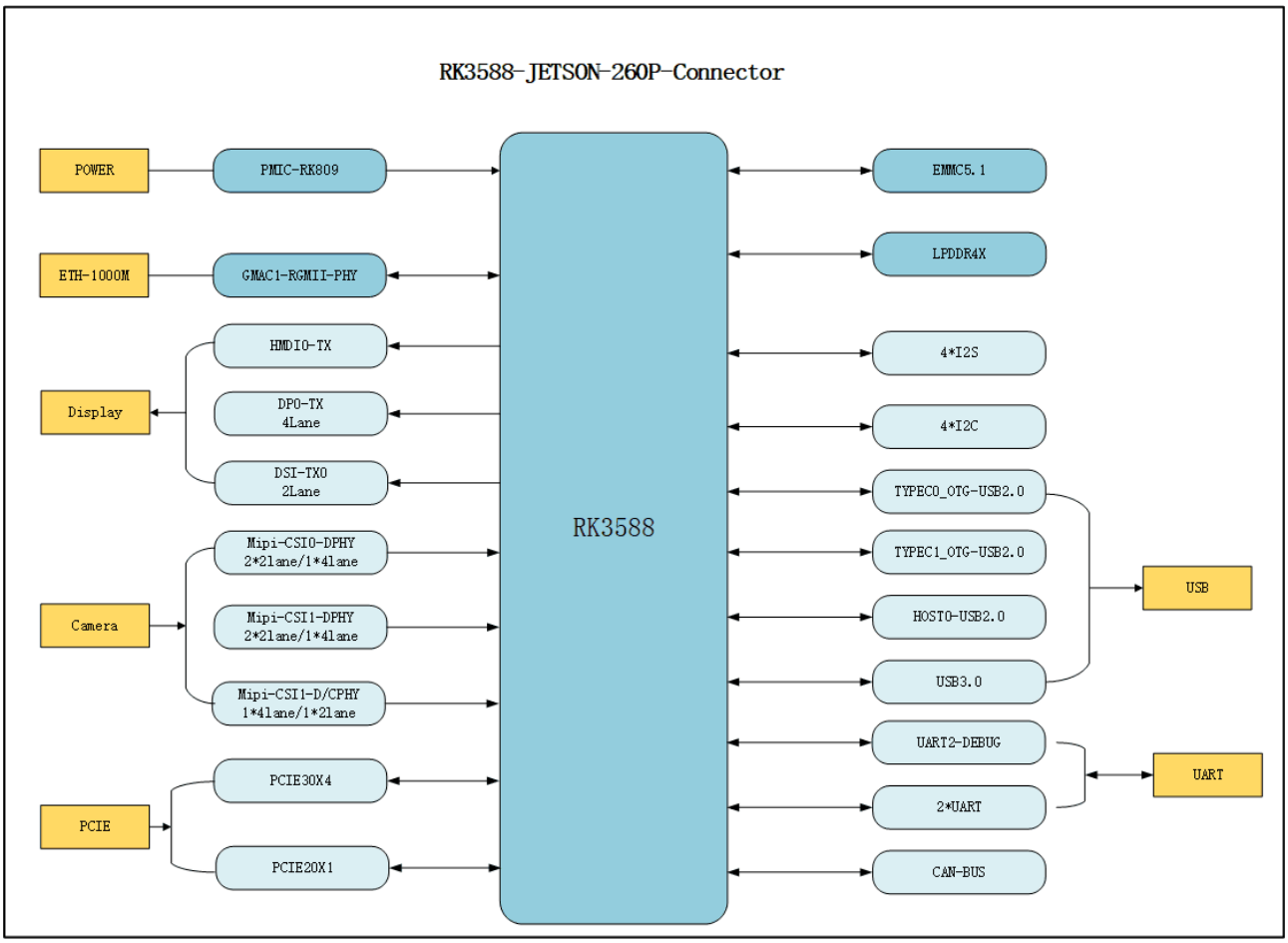
5.5.2 Power Down

Shutdown events can be triggered by either the module or the baseboard, but the shutdown event is always serviced by the baseboard. To do so, the baseboard deasserts POWER_EN, which begins the shutdown power sequence on the module.If the module needs to request a shutdown event in the case of thermal, software, or under-voltage events, it asserts SHUTDOWN_REQ*. When the baseboard sees low SHUTDOWN_REQ*, it should deassert POWER_EN as soon as possible.

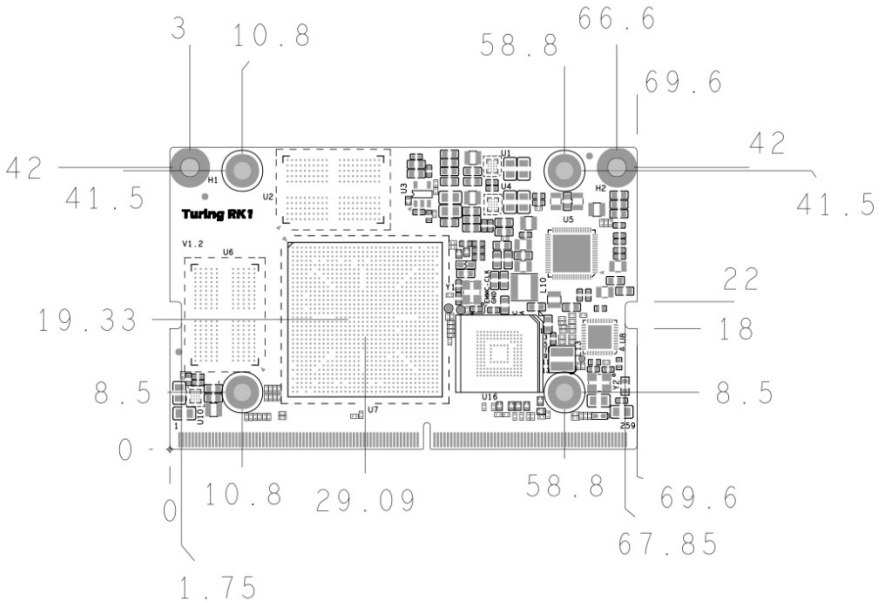
Once POWER_EN is deasserted, the module asserts SYS_RESET*, and the baseboard may shut down. SoC 3.3 V I/O must reach 0.5 V or lower at most 1.5 ms after SYS_RESET* is asserted. SoC

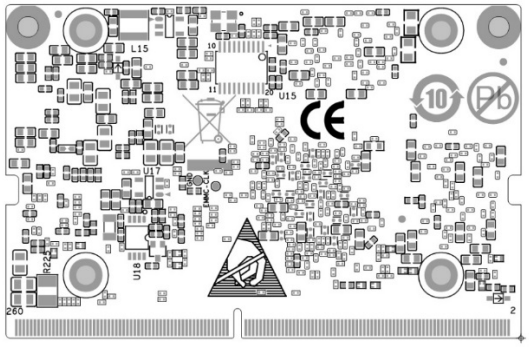
1.8 V I/O must reach 0.5 V or lower at most 4 ms after SYS_RESET* is asserted.

6. Block Diagram



Turing RK1 Dimensional Drawing (Unit:mm)





Board thickness: 1.30mm

7. Pin Definition

The following table lists the pin definition of Turing RK1. For pin comparisons with Jetson Nano/TX2 /NX/Orin.

Turing RK1 Function	Pin Number	Pin Number	Turing RK1 Function
GND_1	1	2	GND_2
MIPI_CSI0_RX_D2N	3	4	MIPI_CSI0_RX_D0N
MIPI_CSI0_RX_D2P	5	6	MIPI_CSI0_RX_D0P
GND_3	7	8	GND_4
MIPI_CSI0_RX_CLK1N	9	10	MIPI_CSI0_RX_CLK0N
MIPI_CSI0_RX_CLK1P	11	12	MIPI_CSI0_RX_CLK0P
GND_5	13	14	GND_6
MIPI_CSI0_RX_D3N	15	16	MIPI_CSI0_RX_D1N
MIPI_CSI0_RX_D3P	17	18	MIPI_CSI0_RX_D1P
GND_7	19	20	GND_8
MIPI_CSI1_RX_D2N	21	22	MIPI_CSI1_RX_D0N
MIPI_CSI1_RX_D2P	23	24	MIPI_CSI1_RX_D0P
GND_9	25	26	GND_10
MIPI_CSI1_RX_CLK1N	27	28	MIPI_CSI1_RX_CLK0N
MIPI_CSI1_RX_CLK1P	29	30	MIPI_CSI1_RX_CLK0P
GND_11	31	32	GND_12
MIPI_CSI1_RX_D3N	33	34	MIPI_CSI1_RX_D1N
MIPI_CSI1_RX_D3P	35	36	MIPI_CSI1_RX_D1P
GND_13	37	38	GND_14
TYPEC0_SSRX1N/DP0_TX0N	39	40	MIPI_DPHY0_RX_D2N
TYPEC0_SSRX1P/DP0_TX0P	41	42	MIPI_DPHY0_RX_D2P
GND_15	43	44	GND_16
TYPEC0_SSTX1N/DP0_TX1N	45	46	MIPI_DPHY0_RX_D0N
TYPEC0_SSTX1P/DP0_TX1P	47	48	MIPI_DPHY0_RX_D0P
GND_17	49	50	GND_18
TYPEC0_SSRX2N/DP0_TX2N	51	52	MIPI_DPHY0_RX_CLKN
TYPEC0_SSRX2P/DP0_TX2P	53	54	MIPI_DPHY0_RX_CLKP

GND_19	55	56	GND_20
TYPEC0_SSTX2N/DP0_TX3N	57	58	MIPI_DPHY0_RX_D1N
TYPEC0_SSTX2P/DP0_TX3P	59	60	MIPI_DPHY0_RX_D1P
GND_21	61	62	GND_22
HDMI_TX2_N	63	64	MIPI_DPHY0_RX_D3N
HDMI_TX2_P	65	66	MIPI_DPHY0_RX_D3P
GND_23	67	68	GND_24
HDMI_TX1_N	69	70	MIPI_DPHY0_TX_D0N
HDMI_TX1_P	71	72	MIPI_DPHY0_TX_D0P
GND_25	73	74	GND_26
HDMI_TX0_N	75	76	MIPI_DPHY0_TX_CLKN
HDMI_TX0_P	77	78	MIPI_DPHY0_TX_CLKP
GND_27	79	80	GND_28
HDMI_TXC_N	81	82	MIPI_DPHY0_TX_D1N
HDMI_TXC_P	83	84	MIPI_DPHY0_TX_D1P
GND_29	85	86	GND_30
GPIO3_C1	87	88	DP0_HPDIN_M1
SPI0_MOSIM2	89	90	TYPEC0_SBU2/DP0_AUXN
SPI0_CLK_M2	91	92	TYPEC0_SBU1/DP0_AUXP
SPI0_MISO_M2	93	94	HDMI_CEC
SPI0_CS0_M2	95	96	HDMI_HPD
SPI0_CS1_M2	97	98	HDMI_DDC_SDA_POL
UART6_TXD_M0	99	100	HDMI_DDC_SCL_POL
UART6_RXD_M0	101	102	GND_31
UART6_RTSn_M0	103	104	SPI2_MOSI_M1
UART6_CTSn_M0	105	106	SPI2_CLK_M1
GND_32	107	108	SPI2_MISO_M1
USB0_OTG_D_N	109	110	SPI2_CS0_M1
USB0_OTG_D_P	111	112	SPI2_CS1_M1
GND_33	113	114	MIPI_CAM3_PDN_L
USB1_OTG_D_N	115	116	MIPI_CAM3_CLKOUT
USB1_OTG_D_P	117	118	GPIO3_C6
GND_34	119	120	MIPI_CAM4_PDN_L
USB2_HOST0_D_N	121	122	MIPI_CAM4_CLKOUT
USB2_HOST0_D_P	123	124	GPIO3_C7
GND_35	125	126	GPIO3_D0/PWM8_M2
GPIO3_D1/PWM9_M2	127	128	GPIO3_D2
GND_36	129	130	GPIO3_D4
PCIE30_PORT0_RX0N	131	132	GND_37
PCIE30_PORT0_RX0P	133	134	PCIE30_PORT0_TX0N
GND_38	135	136	PCIE30_PORT0_TX0P
PCIE30_PORT0_RX1N	137	138	GND_39
PCIE30_PORT0_RX1P	139	140	PCIE30_PORT0_TX1N
GND_40	141	142	PCIE30_PORT0_TX1P
CAN2_RX_M0	143	144	GND_41

CAN2_TX_M0	145	146	GND_42
GND_43	147	148	PCIE30_PORT1_TX2N
PCIE30_PORT1_RX2N	149	150	PCIE30_PORT1_TX2P
PCIE30_PORT1_RX2P	151	152	GND_44
GND_45	153	154	PCIE30_PORT1_TX3N
PCIE30_PORT1_RX3N	155	156	PCIE30_PORT1_TX3P
PCIE30_PORT1_RX3P	157	158	GND_46
GND_47	159	160	PCIE30_REFCLKN_SLOT
TYPEC1_SSRX1N	161	162	PCIE30_REFCLKP_SLOT
TYPEC1_SSRX1P	163	164	GND_48
GND_49	165	166	TYPEC1_SSTX1N
PCIE20_2_RXN	167	168	TYPEC1_SSTX1P
PCIE20_2_RXP	169	170	GND_50
GND_51	171	172	PCIE20_2_TXN
PCIE20_2_REFCLKN	173	174	PCIE20_2_TXP
PCIE20_2_REFCLKP	175	176	GND_52
GND_53	177	178	NC
PCIE30X4/ PCIEX1_1_WAKE_M1	179	180	PCIE30X4_CLKREQ_M1
PCIE30X4_RST_M1	181	182	PCIEX1_1_CLKREQ_M1
PCIEX1_1_RST_M1	183	184	GBE_MDI0_N
I2C5_SCL_M3	185	186	GBE_MDI0_P
I2C5_SDA_M3	187	188	GBE_LED_ACT
I2C4_SCL_M1	189	190	GBE_MDI1_N
I2C4_SDA_M1	191	192	GBE_MDI1_P
I2S0_SDO0	193	194	GBE_LED_LINK
I2S0_SDI0	195	196	GBE_MDI2_N
I2S0_LRCK	197	198	GBE_MDI2_P
I2S0_SCLK	199	200	GND_54
GND_55	201	202	GBE_MDI3_N
UART9_TX_M0_BT	203	204	GBE_MDI3_P
UART9_RX_M0_BT	205	206	GPIO3_D3/PWM10_M2
UART9_RTSn_M0_BT	207	208	SDMMC_DET/GPIO0_A4
UART9_CTSn_M0_BT	209	210	CLK_32K_OUT
GPIO4_B1	211	212	GPIO4_B3
I2C3_SCL_M0	213	214	FORCE_RECOVERY
I2C3_SDA_M0	215	216	GPIO1_A6
GND_56	217	218	GPIO1_A4
SDMMC_DAT0	219	220	I2S2_SDO_M0_BT
SDMMC_DAT1	221	222	I2S2_SDI_M0_BT
SDMMC_DAT2	223	224	I2S2_LRCK_M0_BT
SDMMC_DAT3	225	226	I2S2_SCLK_M0_BT
SDMMC_CMD	227	228	GPIO1_A3/PWM1_M2
SDMMC_CLK	229	230	GPIO1_A2/PWM0_M2
GND_57	231	232	I2C7_SCL_M0_CODEC
NC	233	234	I2C7_SDA_M0_CODEC

RTC_BAT_IN	235	236	UART2_TXD_M0_DEBUG
POWER_EN	237	238	UART2_RXD_M0_DEBUG
SYS_RESET	239	240	NC
GND_58	241	242	GND_59
GND_60	243	244	GND_61
GND_62	245	246	GND_63
GND_64	247	248	GND_65
GND_66	249	250	GND_67
VDD_IN_1	251	252	VDD_IN_2
VDD_IN_3	253	254	VDD_IN_4
VDD_IN_5	255	256	VDD_IN_6
VDD_IN_7	257	258	VDD_IN_8
VDD_IN_9	259	260	NC

8. Technical Support

8.1 contact details : help.turingpi.com